module LDA\_component

(

input clk,

input reset,

input [38:0] avs\_slave\_signals,

input avs\_i\_done,

output avs\_o\_start,

output [2:0] avs\_o\_color,

output [8:0] avs\_o\_x0,

output [7:0] avs\_o\_y0,

output [8:0] avs\_o\_x1,

output [7:0] avs\_o\_y1,

);

logic state;

// state = 0 is stall; state = 1 is poll;

if (!avs\_i\_done && avs\_o\_start) state <= 1’b0;

else state <= 0’b1;

endmodule